REMARKS

Applicants have received the Office action dated July 24, 2006, in which the Examiner rejected claims 1-27 as allegedly unpatentable over Dell et al. (U.S. Pat. No. 6,092,146, hereinafter "Dell") in view of Huang et al. (U.S. Pat. No. 5,008,885, hereinafter "Huang").

Reconsideration is respectfully requested.

I. SECTION 103 REJECTIONS

A. Dell and Huang are not properly considered together.

In attempting to justify considering Dell with Huang, the Office action takes the position that Dell teaches SIMMs memory error insertion, citing Dell's Figure 5 and Column 4, line 55 through Column 5, line 19. (Office action of July 24, 2006, Page 4). However, Dell fails to teach memory error insertion. The cited location is reproduced below for convenience of the discussion.

> Referring, once again, to FIG. 5, once the SIMMs are inserted and the DIP switches are set, the memory adapter of the present invention is inserted into a computer system which requires unbuffered 168-pin DRAM DIMMs. When the computer system is turned on and a Power-On-Reset POR occurs, the logic 500 reads the SIMM presence detects (PDs) and the DIP switch positions in step 502. After step 502, the logic advances to step 504 where it tests to determine if two non-ECC (Error Correction Code) SIMMs are present. ECC generally involves the generation of a special series of bits which code a data byte. The computer system's motherboard or memory adapter must have additional circuitry for producing and comparing the ECC bits for each data transfer. Accordingly, if two non-ECC SIMMs are NOT present, the logic advances to step 506 where EEPROM 106 is turned off. However, if two non-ECC SIMMs are present, EEPROM 106 is programmed via tables 2.1, 2.2, 3.1, 3.2, 4.1, 4.2, and 4.3 by logic device 114 and the I.sup.2 C bus controller 112 in step 508. The programming of EEPROMs is conventional and will not be described hereinafter. After step 508, the logic ends and the EEPROM, if programmed, may now be read by the computer system in the standard way that the Serial Presence Detects (SPDs) are read for DIMMs and the computer system may finish booting normally. In this manner, the logic device 114 serves to program the EEPROM 106 with the required SPDs so as to allow the computer system to properly access the SIMMs. The pin layouts of DIMM and SIMM sockets are conventional and connections there between known. The adapter

> 100 of the present invention includes hardwire connections between the pin configurations of the DIMM socket and the SIMMs.

(Dell Col. 4, line 55 through Col. 5, line 20). While the cited location does discuss ECC bits, the cited location, and Dell in general, fails to teach memory error insertion as suggested by the Office action. Thus, the motivation to consider Dell with Huang discussed in the Office action is without basis, as the primary factor relied upon is the nonexistent memory error insertion of Dell. Huang does not remedy this deficiency of Dell. For this reason alone the rejections should be withdrawn.

B. Claim 1

Claim 1 stands rejected as allegedly obvious over Dell and Huang.

Dell is directed to a dynamically configurable memory adapter using electronic presence detects. (Dell Title). In particular, Dell discloses a memory adapter 100 which allows the use of 72 pin SIMMs in computer systems sporting 168 pin DIMM sockets. (Dell Col. 2, lines 50-55). Huang is directed to an event-controlled error injection system. (Huang Title). In particular, Huang discloses designing the monolithic integrated devices, such as chips 16 and 18, to contain circuitry such that errors can be inserted into the logic from within the chip. (Huang Col. 48-51, Figure 1).

Claim 1, by contrast, specifically recites, "A memory module comprising, a plurality of memory circuits... ; **a plurality of data lines that transfer the data to and from the plurality of memory circuits**; and testing logic coupled to at least one of the plurality of data lines, wherein the testing logic utilizes data stored in the SPD memory circuit to inject a memory error **into one or more of the plurality of data lines**." Applicants respectfully submit that Dell and Huang do not teach or suggest such a system. Huang teaches inserting errors within integrated monolithic integrated circuits. Thus, even if the teachings of Dell are precisely as office action suggests (which Applicants do not admit), Dell and Huang still fail to teach "wherein the testing logic utilizes data stored in the SPD memory circuit to inject a memory error **into one or more of the plurality of data lines**."

Based on the foregoing, Applicants respectfully submit that claim 1 is not rendered unpatentable by Dell and Huang, and that claim 1 should be allowed together with all claims which depend from claim 1 (claims 2-7).

C. Claim 8

Claim 8 stands rejected as allegedly obvious over Dell and Huang.

Dell is directed to a dynamically configurable memory adapter using electronic presence detects. (Dell Title). In particular, Dell discloses a memory adapter 100 which allows the use of 72 pin SIMMs in computer systems sporting 168 pin DIMM sockets. (Dell Col. 2, lines 50-55). Huang is directed to an event-controlled error injection system. (Huang Title). In particular, Huang discloses designing the monolithic integrated devices, such as chips 16 and 18, to contain circuitry such that errors can be inserted into the logic from within the chip. (Huang Col. 48-51, Figure 1).

Claim 8, by contrast, specifically recites, "receiving a request to inject an error **into a data line** of a memory module; and injecting the error **into the data line** by a testing logic integrated with the memory module." Applicants respectfully submit that Dell and Huang do not teach or suggest such a system. Huang teaches inserting errors within integrated monolithic integrated circuits. Thus, even if the teachings of Dell are precisely as office action suggests (which Applicants do not admit), Dell and Huang still fail to teach "injecting the error **into the data line** by a testing logic... "

Based on the foregoing, Applicants respectfully submit that claim 8 is not rendered unpatentable by Dell and Huang, and that claim 8 should be allowed together with all claims which depend from claim 8 (claims 9-15).

D. Claim 16

Claim 16 stands rejected as allegedly obvious over Dell and Huang.

Dell is directed to a dynamically configurable memory adapter using electronic presence detects. (Dell Title). In particular, Dell discloses a memory adapter 100 which allows the use of 72 pin SIMMs in computer systems sporting 168 pin DIMM sockets. (Dell Col 2, lines 50-55). Huang is directed to an event-controlled error injection system. (Huang Title). In particular, Huang discloses

designing the monolithic integrated devices, such as chips 16 and 18, to contain circuitry such that errors can be inserted into the logic from within the chip. (Huang Col. 48-51, Figure 1).

Claim 16, by contrast, specifically recites, "applying a bias voltage on at least one data line associated with the error injection procedure." Applicants respectfully submit that Dell and Huang do not teach or suggest such a system. Huang teaches inserting errors within integrated monolithic integrated circuits. Thus, even if the teachings of Dell are precisely as office action suggests (which Applicants do not admit), Dell and Huang still fail to teach "applying a bias voltage on at least one data line associated with the error injection procedure."

Based on the foregoing, Applicants respectfully submit that claim 16 is not rendered unpatentable by Dell and Huang, and that claim 16 should be allowed together with all claims which depend from claim 16 (claims 17-20).

E. Claim 21

Claim 21 stands rejected as allegedly obvious over Dell and Huang.

Dell is directed to a dynamically configurable memory adapter using electronic presence detects. (Dell Title). In particular, Dell discloses a memory adapter 100 which allows the use of 72 pin SIMMs in computer systems sporting 168 pin DIMM sockets. (Dell Col. 2, lines 50-55). Huang is directed to an event-controlled error injection system. (Huang Title). In particular, Huang discloses designing the monolithic integrated devices, such as chips 16 and 18, to contain circuitry such that errors can be inserted into the logic from within the chip. (Huang Col. 48-51, Figure 1).

Claim 21, by contrast, specifically recites, "a plurality of means for transferring data to and from the plurality of means for storing data; and a means for applying a bias voltage coupled to the plurality of means for storing data, wherein the means for applying a bias voltage utilizes data stored in the SPD memory circuit **to inject an error into at least one of the plurality of means for transferring data**." Applicants respectfully submit that Dell and Huang do not teach or suggest such a system. Huang teaches inserting errors within integrated monolithic integrated circuits. Thus, even if the teachings of Dell are precisely as

office action suggests (which Applicants do not admit), Dell and Huang still fail to teach "wherein the means for applying a bias voltage utilizes data stored in the SPD memory circuit **to inject an error into at least one of the plurality of means for transferring data**."

Based on the foregoing, Applicants respectfully submit that claim 21 is not rendered unpatentable by Dell and Huang, and that claim 21 should be allowed together with all claims which depend from claim 21 (claims 22-27).

II. CONCLUSION

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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